

Characterization of a Thick Copper Pillar Bump Process

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Abstract

As pin counts and interconnection densities increase there is growing interest in copper pillar bumps for flip chip and wafer-level packaging. This trend is driven by the need to increase interconnect performance as well as reduce interconnect cost. Copper pillars retain their shape during solder reflow, allowing finer interconnect pitches with predictable standoff heights. The fabrication of copper pillar bumps requires the use of a very thick photoresist layer for copper and nickel electroplating. This photoresist material must be capable of coating, exposing, developing, electroplating and stripping with conventional track equipment and standard ancillary process chemicals. For the electroplating process the photoresist profile, plating durability and stripability are important considerations.

This study will characterize a photoresist for a single coat, 55 μm thick copper process. The lithographic performance of the thick positive photoresist will be optimized using a broad band, low numerical aperture stepper. Results will show good adhesion to copper with no surface treatment and no photoresist cracking during plating. Cross sectional SEM analysis, process latitude, and copper-nickel electroplating performance are used to establish the lithographic capabilities.

Introduction

As pin counts and interconnect densities continue to increase, there is growing interest in copper pillar bumps as an alternative to conventional solder bumps for flip chip and wafer-level packaging. Copper pillar bumps were first introduced into production by Intel in 2006 [1]. Numerous wafer bump foundries and semiconductor manufacturers are now actively evaluating this technology.

The increasing interest in copper pillar bumps is part of an overall trend from packaging devices using wire bonding to flip chip packaging and wafer-level packaging. Although the large majority of all devices are still packaged using wire bonding, flip chip packaging is gaining acceptance for high-end devices that are performance driven, while wafer-level packaging is gaining acceptance for low input/output (I/O) devices that are form factor driven, as shown in Figure 1 [2].

The use of flip chip packaging continues to expand as flip chip reaches cost parity with wire bonding in many applications. At the low I/O end, wafer-level packaging is now being adopted for memory, as shown in Figure 2 [2].

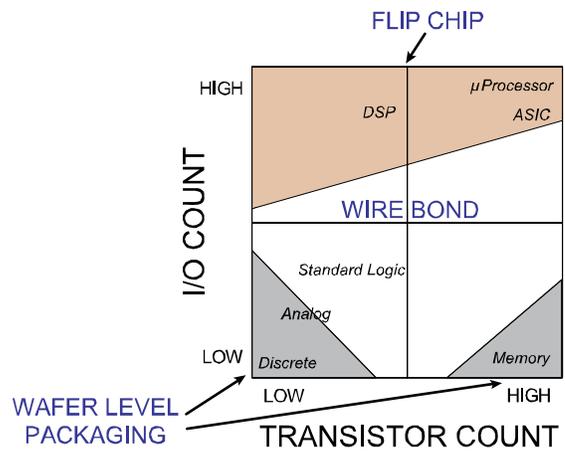


Figure 2: Current view of packaging technology

Copper pillar bumping represents the high end of this trend, which can be performance-driven, form factor driven or potentially both.

Copper pillars offer numerous advantages over solder bumps for flip chip packaging and wafer-level packaging [3]. These advantages include higher interconnect densities, higher reliability, improved electrical and thermal performance, and reduction or elimination of lead. Conventional solder bumps use “mushroom” overplating as shown in Figure 3. While solder bumps collapse during solder reflow, copper pillars retain their shape in the x, y and z directions. This allows the fabrication of finer bump pitches, smaller passivation openings, and finer redistribution wiring for higher interconnect densities. Eliminating bump collapse also enhances reliability due to more uniform bump pitch and standoff distances. During the assembly process, underfill applied between the die and substrate tends to flow more easily into the larger gaps, with voids left in the smaller gaps.

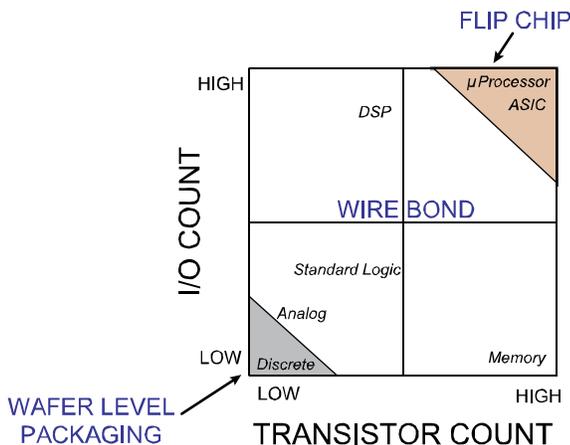


Figure 1: Historical view of packaging technology

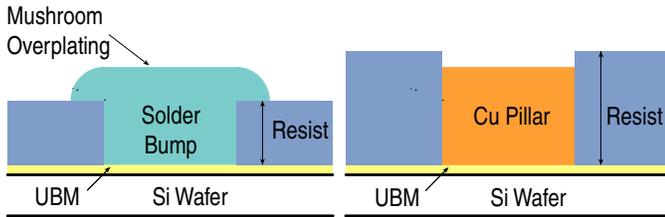


Figure 3: Comparison of Mushroom solder and copper pillar processes

More uniform bump pitch and standoff distances facilitate more complete underfill and, ultimately, higher component reliability [4]. Copper pillars are also inherently capable of higher aspect ratios than solder bumps. Larger standoff heights may also improve reliability by reducing strains caused by coefficient of thermal expansion (CTE) differences between the die and substrate [5]. By virtue of their reduced lead-content, copper pillars also offer advantages with respect to better electrical and thermal conductivity, as well as increased electromigration resistance and current carrying capability [6]. Finally, copper bumping allows closer compliance with the restriction of hazardous substances (RoHS) regulations, although the process may not be completely lead-free if the pillars are capped with a leaded solder.

The objective of this study is to evaluate the lithography processes required to fabricate thick copper pillar structures. A thick photoresist layer is required to act as a mold for the copper electroplating. Typical photoresist thicknesses are in the 40 to 100 μm range, which is thicker than for solder bumping.

The photoresist material must be capable of coating, exposing, developing, electroplating and stripping with conventional equipment and standard ancillary process chemicals. For the electroplating process the photoresist profile, plating durability and stripability are important considerations [7]. Furthermore, the choice of a positive photoresist is important to obtain the process advantages of a dark field mask [8].

This study utilizes a positive acting, chemically amplified, photoresist for a single coat thick copper process. This photoresist has been formulated for post electroplating stripability and has additives to eliminate the cracking often encountered with electroplating using thick films. Lithography for the thick positive photoresist is performed using a broad band, low numerical stepper. Cross sectional SEM analysis, imaging process latitude, and copper electroplating performance are used to validate the lithographic processes. The overall process margin is compared to current and future copper pillar requirements.

Experimental Methods

Lithography for this study was performed using an Ultratech Unity AP300 Wafer Stepper. This system has a 0.16 numerical aperture (NA) and employs Mercury ghi-line illumination from 350 to 450 nm. The low NA and broadband illumination spectrum of the stepper provides a large depth of focus and minimizes the standing wave pattern in the photoresist side wall near the substrate [9]. The exposure dose

and focus offsets of the stepper were optimized for 50 μm contacts in the photoresist. A wafer edge exposure (WEE) system was used to create a photoresist free area around the edge of the wafer for electrical contact during plating [10].

Two reticles were used in this study. The first reticle was designed for cross sectional SEM metrology to establish the process window. This reticle consists of a 10 by 10 mm field containing line and square contact patterns from 40 μm to 100 μm in size. A second reticle used for electroplating. It has a 37 mm by 15.5 mm field size and contains 30 μm to 100 μm round contacts with various pitches.

SEMI standard 200 mm prime copper seed wafers were used for this study. The photoresist used is Shin-Etsu SIPR 7126M-20. The photoresist was coated to the 55 μm target thickness using the process and equipment described in Table 1. No additional adhesion promoter was used. Photoresist thickness and uniformity was measured on a Steag ETA Optik thickness measurement tool.

The photoresist is a TMAH developable, chemically amplified, positive photoresist. The thickness at 3000 rpm is 20 μm and can be coated up to 55 μm thick in a single application. TMAH 0.26N developer without surfactant was used in the experiment. Even though the photoresist is i-line sensitive, no wavelength filtering was needed. The exposure wavelength selected was ghi-line of mercury. Post Exposure Bake (PEB) is not required. The development method is immersion at room temperature, followed by a DI water rinse.

Process Step	Parameters	Equipment
Coat	pre-wet: Fujifilm RER 600 for 10 sec Dry at 1400 rpm for 1 second Static dispense for 16 seconds Spread: 500 rpm for 5 seconds Spin: 480 rpm for 80 seconds Backside Rinse: 480 rpm for 20 sec Dry: 480 rpm for 10 seconds	ACS 200
Softbake	Hotplate, 0.2 mm proximity 2 minutes at 90°C 8 minutes at 130°C	ACS 200
Exposure	ghi-line, focus-exposure matrix 1.5 mm WEE PEB: not required	AP 300
Develop	7 min immersion 2.38% TMAH, 21°C Constant and aggressive agitation DI water rinse Spin rinse and dry	

Table 1: The lithography process used for 55 μm thick photoresist on 200mm copper wafers.

For electroplating, the wafers were processed at nominal conditions (1400 mJ/cm^2 at -10 μm focus, ghi wavelength) with an wafer edge width exposure of 1.5 mm. For pillar formation copper electroplating was followed by nickel electroplating. Copper electroplating was performed using a Microfab Cu-200 for 15 minutes at room temperature and nickel was done using a Microfab Ni-200 for 60 minutes at 55°C. After electroplating the photoresist was stripped by soaking in acetone for 10 minutes at room temperature.

Multiple wafers were exposed in a focus/exposure pattern [8]. After exposure the wafers were cleaved for cross section

on a Joel JSM 6340F and Hitachi S7280 metrology SEM to show linearity and depth of focus of 50 μm spacewidths and square contacts. Bottom CD measurements were taken for 50 μm square contacts to show depth of focus at nominal exposure and linearity at nominal exposure and focus. Cross sectional SEM photographs and Bossung plots are presented to illustrate masking linearity and depth of focus at nominal exposure dose.

Lithography Results and Discussion

The first step for lithography optimization is to set up a baseline photoresist process to support copper electroplating. This was initially done using dense line and space patterns. This pattern offer an advantage over contacts in that it can be easily cleaved and critical dimensions (CD) measured using a SEM. Figure 4(a) shows the spacewidth process linearity for 55 μm thick photoresist on copper substrates in a dense line and space pattern. The lithography conditions are 1400 mJ/cm^2 (ghi-line exposure) with a -10 μm focus offset. This graph shows that the printed feature size is linear with respect to the reticle feature size.

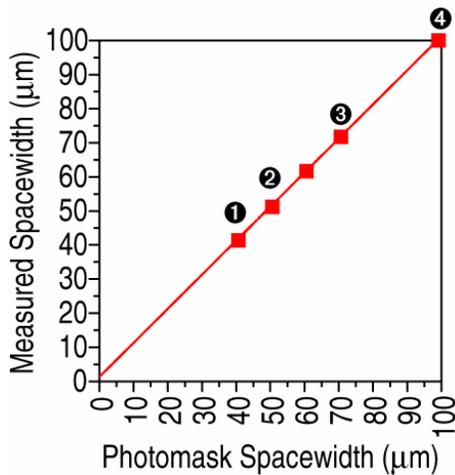


Figure 4(a): Mask linearity for spacewidth in 55 μm thick photoresist on copper substrates

This plot was constructed using cross-sectioned SEM data for spacewidth and is a best fit plot of the data to the equation:

$$y = x + b \quad (1)$$

In this equation, y is the measured spacewidth, x is the reticle spacewidth and b is the photomask bias. The photomask bias is 1.261 μm with an R^2 data fit of 0.999. Typically positive photoresists in this thickness range would have a larger photomask bias [7]. A small reticle bias is a process advantage since it can simplify reticle design and fabrication. Figure 4(b) shows cross sectional SEM photographs of the process linearity for 40, 50, 70 and 100 μm spacewidths. The number in the black circle below each photograph matches the number in Figure 4(a). The sidewall angle is nearly vertical for all space widths. Very little rounding is observed at the top of the photoresist. This implies that the copper can be electroplated to the full photoresist thickness and still maintain control of the pillar profile. This is important factor for minimizing spacing of pillars to support high interconnect density. In addition, no footing was observed which can lead to underplating and weaker pillar strength.

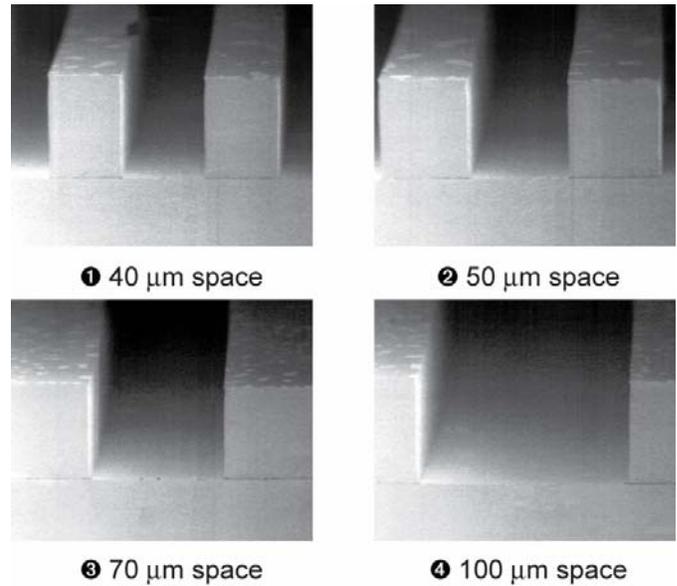


Figure 4(b): SEM photographs of spacewidth linearity at 1400 mJ/cm^2 (ghi-line exposure) and -10 μm focus offset.

The baseline process for lines and spaces can now be used to optimize the lithography process for the contact structures that are to be copper electroplated. Figure 5(a) shows the

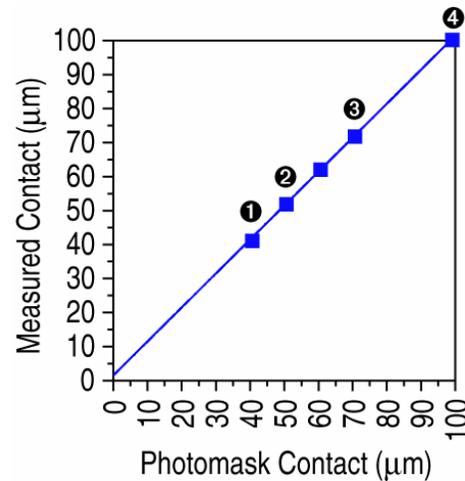


Figure 5(a): Mask linearity for dense square contacts in 55 μm thick photoresist on copper substrates.

process linearity for 55 μm thick photoresist on copper substrates for a dense array of square contacts patterns. The process conditions are 1400 mJ/cm^2 (ghi-line exposure) with a -10 μm focus offset. The photomask bias is +1.46 μm with an R^2 data fit of 0.999. The reticle bias for the contacts is slightly larger than that observed for the spacewidth.

Figure 5(b) shows cross sectional SEM photographs of the process linearity for contacts at 40, 50, 70 and 100 μm . The number in the black circle below each photograph matches the number in Figure 5(a). The process conditions are 1400 mJ/cm^2 (ghi-line exposure) with a -10 μm focus offset. The sidewall angle is comparable with the sidewall observed for the spacewidth patterns. This indicates that there is minimal pattern effect for the photoresist process and no focus or exposure dose was need for pattern type. The observed resolution of 40 μm exceeds the contact size for copper pillars

currently being considered for advanced packaging applications. This resolution provides for a wider margin of CD control required for a manufacturing process.

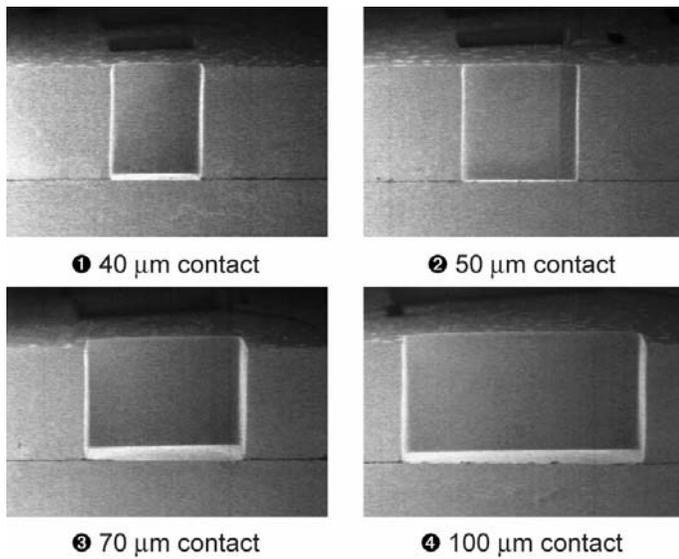


Figure 5(b): SEM photographs of contact linearity at 1400 mJ/cm² (ghi-line) and -10 µm focus offset.

The process latitude of 50 µm square contacts were evaluated by measured the CD variation through focus and exposure dose. Figures 6 show a graphical analysis of CD variation using a Bossung plot. The vertical axis is the measured contact CD and the horizontal axis shows the focus offset from -20 µm to +20 µm. The exposure dose is shown using multiple curves for exposure doses from 1200 to 1800 mJ/cm² (ghi-line exposure). The two horizontal grey lines in the plot show a five percent CD control limit for the 50 µm contacts. At 1600 mJ/cm² and higher the exposure dose curves fall out of the five percent CD control limit for focus offsets larger than zero. However, for 1400 mJ/cm² and smaller the exposure dose curves stay within the CD limits over nearly the entire focus range. This large focus latitude can be advantageous for controlling CD over local topography variations on product wafers.

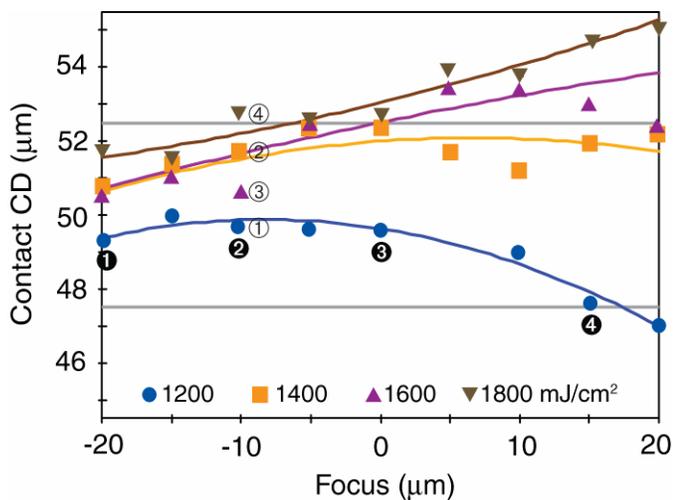


Figure 6: Bossung plot of 50 µm contacts in 55 µm thick photoresist on copper substrates.

Figure 7(a) shows cross sectional SEM photographs of 50 µm contacts through focus in 55 µm thick photoresist on copper substrates. The number in the black circle below each photograph matches the numbers in the Bossung plot (Figure

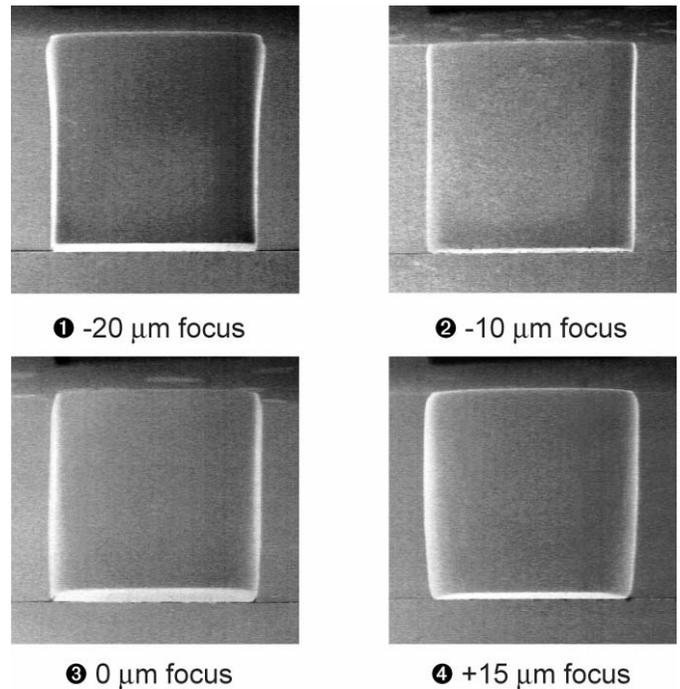


Figure 7(a): SEM photographs of 50 µm square contacts through focus.

6). The -20 µm focus offset in figure 1 shows some rounding at the top of the photoresist. In contrast the +15 µm focus offset in figure 4 shows a moderate foot at the bottom of the photoresist. The best compromise between the footing and the top rounding is a focus offset of -10 µm as shown in figure 2. Also at this optimum exposure and focus condition the photomask print bias is extremely small as shown in Figure 6.

Figure 7(b) shows cross sectional SEM photographs of 50 µm contacts through exposure dose in 55 µm thick photoresist on copper substrates. The number in the white circle below each photograph matches the numbers in the Bossung plot (Figure 6). The 1600 and 1800 mJ/cm² exposure doses in figures 3 and 4 show a convex shaped bowing in the photoresist sidewall. This bowing causes the CD to be larger at the bottom of the photoresist. This is a reason that the higher exposure dose curves in Figure 6 above of the five percent CD control limits. In contrast, the 1200 and 1400 mJ/cm² exposures doses in figures 1 and 2 show near vertical photoresist sidewalls. Based on these results the optimal process conditions for CD are 1400 mJ/cm² and -10 µm focus.

The process latitude of 50 µm square contacts can also be evaluated by measuring the sidewall angle of the photoresist. Control of the sidewall angle is critical for the copper electroplating operation. Figure 8 shows a graphical analysis

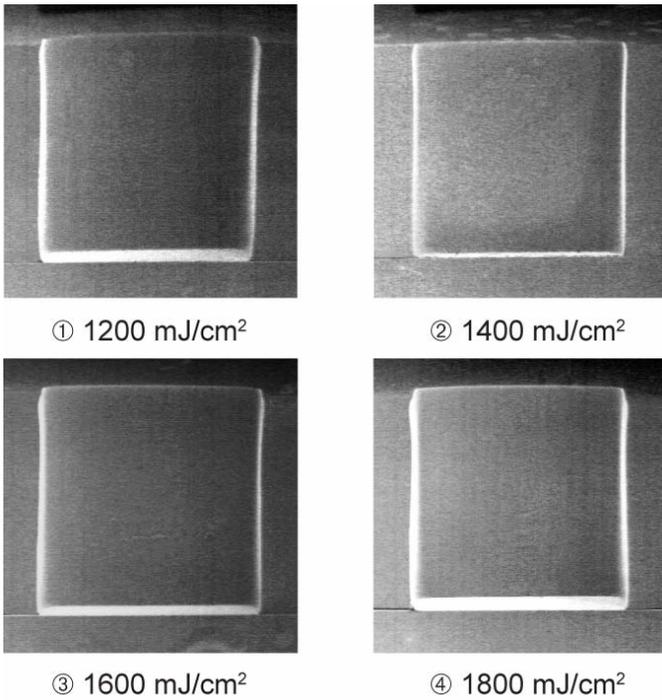


Figure 7(b): SEM photographs of 50 μm square contacts through exposure dose (ghi-line exposure).

of sidewall angle using a process window plot [8]. The envelope region outlined in bold shows a sidewall angle of 88° or larger. The shaded box is the largest rectangular process window providing the maximum exposure dose range that fits within the envelope region. Other rectangles can be drawn in the envelope region depending on exposure and focus latitude requirements for a given process. The previously selected process conditions for optimal CD control of exposure dose of 1400 mJ/cm^2 and the focus of $-10 \mu\text{m}$ is shown by a black dot. It is located well within the specified 88° sidewall angle process window.

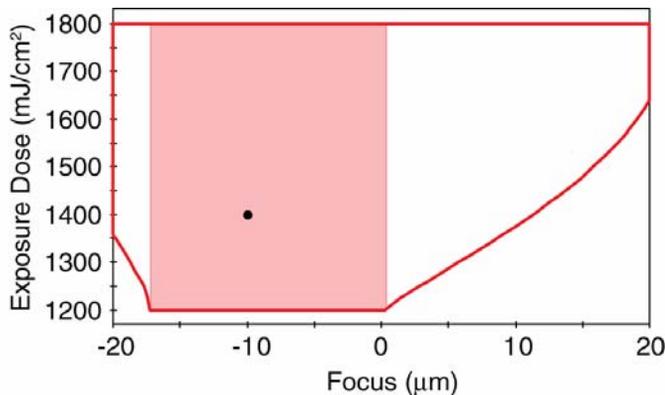


Figure 8: Process window of 50 μm square contacts with an 88° sidewall angle criterion.

Electroplating Results and Discussion

The electroplating performance of the patterned photoresist is extremely critical for copper pillar formation. There are two major factors in regards to the electroplating: durability and stripability. The photoresist needs to be durable enough to withstand multiple plating solutions that might have different pH values, different temperatures and

different plating rates. For pillar electroplating it is typical to plate copper followed by nickel or titanium. A consequence of designing a photoresist for this kind of durability is that they are typically difficult to strip after electroplating, and often require aggressive, non environment-friendly solvents like NMP.

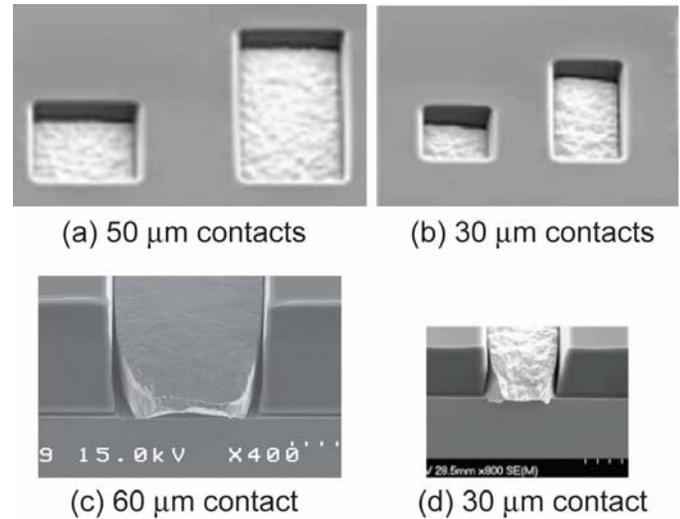


Figure 9: SEM photographs after copper and nickel electroplating, but before removal of the photoresist. The total plating thickness is $30.0 \mu\text{m}$.

Angled SEM photographs of copper and nickel electroplated 50 and 30 μm contacts before photoresist stripping are shown in Figures 9 (a) and (b). There is no indication of photoresist cracking in these photographs. Typically, if there is cracking in the photoresist, there will be hairline cracks emanating from the corners of the square contacts. Cross sectional SEM photographs of 30 and 60 μm electroplated contacts before photoresist stripping are shown in Figures 9 (c) and (d). These photographs show good adhesion to copper with no visible signs of underplating.

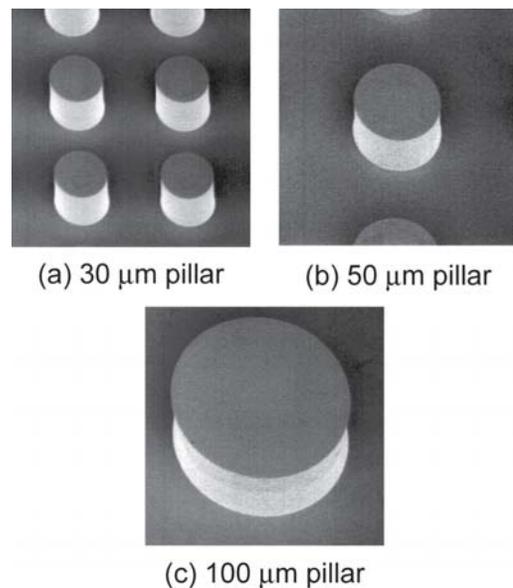


Figure 10: SEM photographs of round copper pillar CD linearity.

SEM photographs are used to determine the CD linearity of the final electroplated copper pillar structures. Figure 10 shows round copper pillars from 30 to 100 μm in 55 μm thick photoresist on copper seed substrates. The average pillar height is 30.0 μm as measured using a Dektak V300-Si. The pillars show vertical sidewall profiles with no signs of underbump electroplating. The photoresist demonstrated adequate durability in the electroplating bath with no adhesion failure.

Cross sectional SEMs are used to show grouped and isolated electroplated 50 μm copper pillar structures. Figures 11 shows round copper pillars from 12.5 μm spacing (4:1 ratio) to 100 μm spacing (1:2 ratio) in 55 μm thick photoresist on copper seed substrates. There is no indication of copper bridging between bumps.

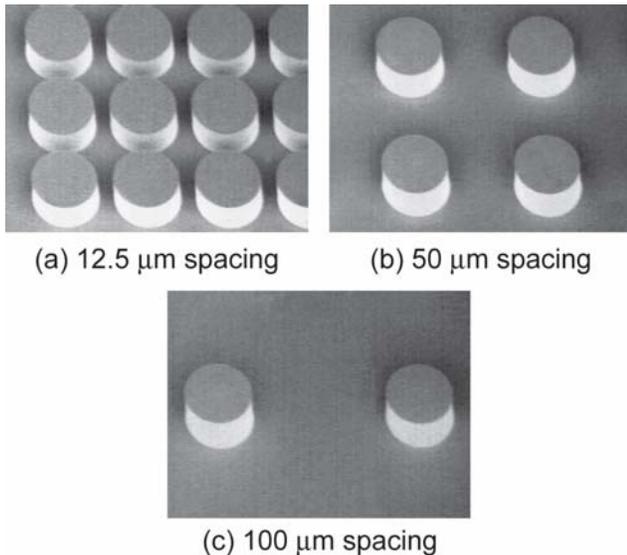


Figure 11: SEM photographs grouped and isolated electroplated 50 μm diameter copper pillar structures.

Conclusions

The objective of this study was to characterize a lithography process for a current generation copper pillar application. A positive tone, non-PEB, chemically amplified photoresist was shown to have adequate resolution, process latitude, electroplating and stripping performance. No photoresist cracking was observed after copper and nickel electroplating. In addition good adhesion with no underplating was observed. The lithography and electroplating performance meets the requirements for current generation copper pillar processing and shows latitude to meet the expected requirements in the future.

Acknowledgments

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