

LITHOGRAPHY CHALLENGES FOR LEADING EDGE 3D PACKAGING APPLICATIONS

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ABSTRACT

Leading edge consumer electronic products drive demand for enhanced performance and small form factors. This in turn drives manufacturing requirements for all aspects of semiconductor device fabrication. As the cost of front end device manufacturing continues to escalate rapidly with each new technology node, semiconductor manufacturing companies are now also focusing on packaging technology to deliver improved performance and reduced form factor. A number of innovative technologies are being developed to support increasing packaging density requirements. It is anticipated that advanced three dimensional (3D) packaging technologies such as TSV (Through Silicon Via) manufacturing will play a critical role in future semiconductor device miniaturization. Advanced system in package (SiP) capability is now viewed as a key strategic technology by device manufacturers and foundry companies. Several SiP techniques will require TSV to provide high density vertical interchip wiring of multiple device stacks. These vias need to be freely placed in the device which creates a requirement for tight registration of the back-to-front side device alignment. This paper investigates the lithography challenges associated with TSV fabrication for various devices structures.

Silicon test wafers have been fabricated with a variety of films to evaluate the back-to-front side wafer alignment. The reference layer is defined in a standard damascene copper process and protected with a passivation layer. Next the wafers are flipped, bonded, and thinned to various thicknesses. Some wafers are also processed through a chemical mechanical polish (CMP) step. The importance of surface quality is analyzed since CMP is required to create an optically smooth surface and this processing step is expensive which impacts overall fabrication cost. Images of the embedded alignment target are shown for various silicon thicknesses and wafer surface quality. Experimental back-to-front alignment metrology data is shown as a function of silicon thickness for various film stacks.

Key words: Overlay, 3D Packaging, TSV, SiP

INTRODUCTION

Advanced packaging technologies have become increasingly important as semiconductor device manufacturers are transitioning to next generation front end technology nodes. With the escalating cost of manufacturing front end silicon wafers, both device manufacturers and foundry customers are considering the use of innovative 3D packaging technologies to meet product performance in a cost effective fashion. One such technology is the adoption of TSV manufacturing.

The use of TSV technology was first commercialized by CMOS image sensor manufactures for use in high end mobile phones [1]. It is expected that memory companies will start utilizing TSV technology for stacking memory chips to meet the high data rate transfer requirements within the next few years [2]. As the industry and equipment infrastructure becomes more robust, it is also expected that this technology will also be utilized for mixed device integration. Since the use of packaging technology to deliver improved price to performance ratio is novel, it places unique challenges for the entire supply chain. As such device manufacturers, wafer foundries and packaging foundries are now utilizing production proven equipment solutions to meet the high volume requirements.

Lithography is one of the critical process steps that affect the final device performance and associated yield for TSV manufacturing. One of the unique lithography challenges during TSV process step is the need for back-to-front side alignment solution. This challenge arises from the fact that the 3D devices have active metallization levels on both sides of the device and when patterning the back side, the front side alignment targets are not visible using conventional alignment approaches.

The industry is evaluating three different approaches to device and TSV co-integration that can be classified according to where in the process flow the TSV is patterned and filled. They are called via first, via middle and via last depending on whether the TSV is integrated before front-end-of-line (FEOL), after FEOL but before back-end-of-line

BEOL, or after BEOL [3,4,5]. For the TSV via last process the device wafer is thinned, polished, and then mounted on a carrier with the device side against the carrier. In doing so, the original front side of the wafer becomes an embedded layer as shown in figure 3. The naming convention used in this study is that the wafer device side is the front side and the silicon side is the back side. The side facing up on the stepper is the back side of the TSV wafer.

ALIGNMENT SYSTEM

The embedded lithography alignment target can be viewed using three different techniques as shown in figure 1. These are direct view alignment using prisms embedded in the wafer chuck (a), illuminating with infrared (IR) light source embedded in the wafer chuck (b), and illuminating with IR light from the top (c). Both direct view alignment system and IR illumination from the wafer chuck result in constraints with respect to location of alignment targets on the wafer which reduces the operational flexibility. Top IR illumination of the wafer gives the most robust manufacturing solution for TSV manufacturing. Imaging of embedded targets through silicon relies on the property of silicon that it is transparent for IR wavelengths. For top illumination the target needs to be made from a reflective material such as metal for best contrast.

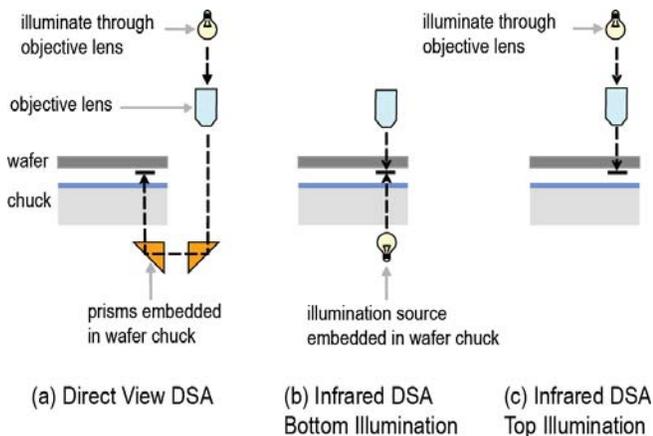


Figure 1: Three different techniques for viewing an embedded target for back-to-front side alignment.

The lithography system used in this investigation implements a topside IR illumination configuration for back-to-front side alignment which provides flexibility in target number and placement on a 300mm wafer. The back-to-front side system, or dual side alignment (DSA) application was originally developed for CMOS image sensor applications [6]. This application required alignment to embedded metal targets below silicon, and the system was designed to achieve back-to-front side overlay of less than $2 \mu\text{m}$ ($|\text{mean}| + 3\sigma$) over a full 300mm wafer. These capabilities meet the current requirements for TSV via last process. Unlike many front side alignment systems which view the wafer through the projection lens (TTL), the DSA alignment system views the wafer in an off-axis configuration. Therefore the calibrated offset between the

exposure and alignment systems is maintained using a common stage fiducial that is measured by both DSA and TTL alignment systems.

Figure 2 compares conventional front side alignment and via last TSV alignment. The non-TSV off axis alignment for front side exposures is shown in figure 2(a). Since the focal planes for alignment and exposure systems are coincident, the wafer does not need to move much in Z to perform front side processing. The off axis alignment and exposure of an embedded target for the via last TSV process is shown in figures 2(b) and 2(c) respectively. Here a large Z move is required for DSA to an embedded target since the focal planes for alignment and exposure are separated. Note that since silicon has a large index of refraction in the near IR of 3.5, the required Z offset is less than the silicon thickness.

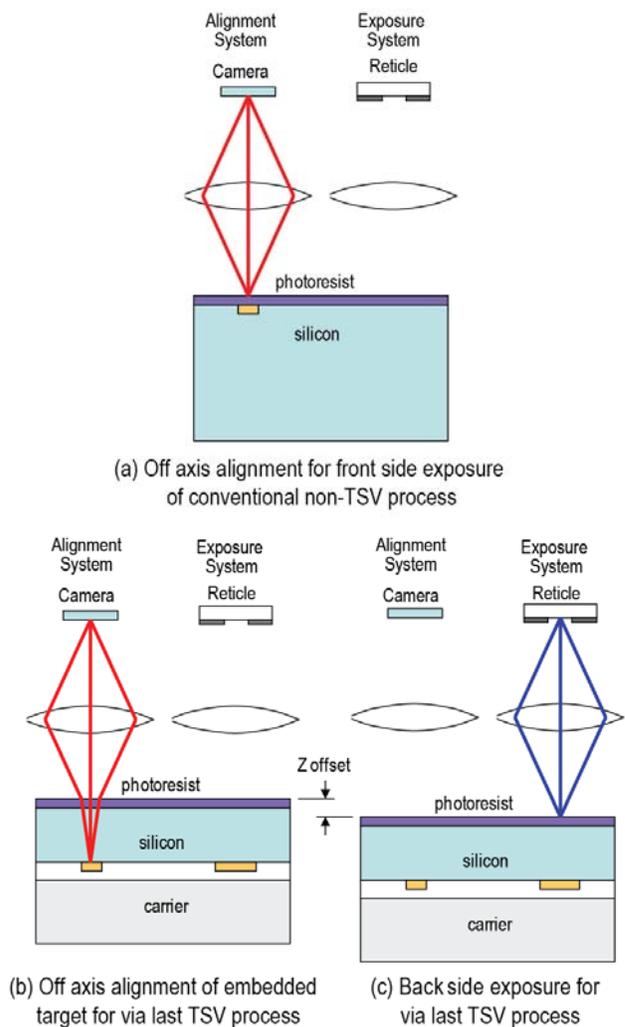


Figure 2: Alignment and exposure sequence for via last TSV application using an off-axis IR DSA camera. (a) Conventional alignment for a front side non-TSV process, (b) alignment of embedded target for via last TSV, (c) back side exposure for via last TSV. Note that regardless of orientation, the wafer device side is referred as the front side and the silicon side is the back side.

EXPERIMENTAL METHODS

The lithography system used for back-to-front side alignment is an Ultratech AP300 DSA. The stepper has a 0.16 NA, 1X Wynne-Dyson projection lens design, illuminated by broadband g-line illumination [7,8]. The stepper is used in high volume advanced packaging applications and provides a stable platform for DSA operation. In this investigation two types of overlay tests were run on 200 mm wafers.

Single Pass Topside Overlay Test

The first test, denoted as a single pass topside overlay, has alignment and metrology features etched in the top silicon surface. The single pass topside test is used for baseline monitoring of stepper overlay performance. The base pattern wafers were created using an ASML PAS5500/750 deep UV scanner with a specially designed mix-and-match test reticle containing alignment targets and various metrology structures. These patterns were then etched 500 nm into the silicon surface to make artifact wafers. Baseline monitoring for the single pass test can be performed using a variety of automated metrology systems which are optimized for topside planar structures.

A complementary mix-and-match test reticle was used on the AP300 for single pass testing. Alignment of targets at the top surface of the wafer was performed using the off axis DSA camera. The photoresist was 1800nm thick IX845 exposed at $250\text{mJ}/\text{cm}^2$ in i-line mode. The IX845 photoresist was coated and developed on a TEL ACT12 track. The resulting exposure wafers can be measured using conventional overlay metrology tools.

Double Pass Embedded Overlay Test

Obtaining precise metrology for measuring back-to-front side overlay performance is an industry challenge. Unlike front side wafer processing where automated metrology tools are widespread, metrology options are limited for back-to-front side overlay. The double pass test is specifically designed to take advantage of existing metrology capabilities. This technique measures overlay from embedded target alignment by forming structures at the top surface that can be measured using conventional topside metrology [6].

The double pass test wafers were prepared using a copper damascene process. A dielectric layer consisting of 250 nm of SiO_2 was deposited followed by an etch-stop layer and 600 nm of SiO_2 . Then a PAS5500/750 scanner was used to image a base pattern using a specially designed mix-and-match test reticle. After etching the 600 nm SiO_2 layer, 1000 nm of copper was deposited to fill the trenches and Chemical Mechanical Polish (CMP) was used to expose the underlying oxide, leaving a flat surface with copper filled trenches. This was covered by a SiO_2 passivation layer.

The copper damascene wafers were inverted and glued to a silicon carrier. The wafers were thinned using a grinding system to three Si thicknesses (100, 200, and 300 μm). The

last step was polishing the surface by CMP to remove surface damage leaving an optically smooth surface. The TTV (Total Thickness Variance) of the wafers was measured to be below 3 μm . The resulting wafer cross section is shown in figure 3. One double pass artifact wafer was left un-polished to evaluate the impact of the grinding scratches on the embedded target capture quality.

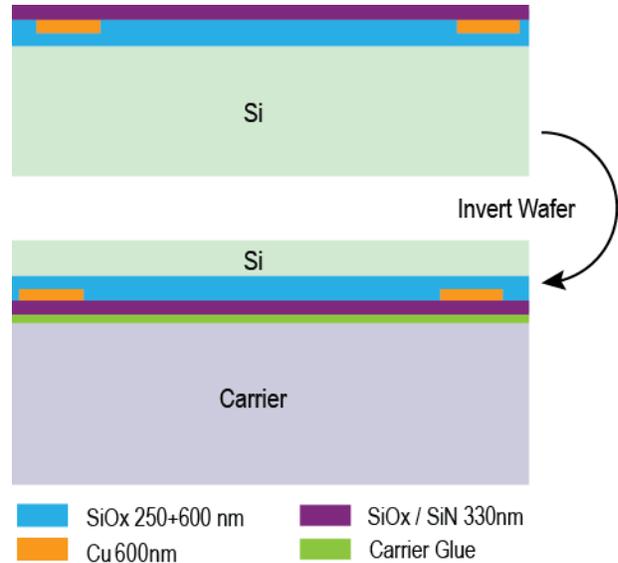


Figure 3: Cross section of test wafers with embedded damascene Cu targets. Wafers are inverted, glued to a carrier, and then the silicon is thinned and polished.

A mix-and-match test reticle designed to match the PAS 5500/750 patterns was used on the AP300 for double pass testing. Two layers are sequentially aligned and exposed: the first layer is aligned to the embedded reference target and with the wafer oriented at 0° rotation, and the second layer is aligned and exposed with the wafer oriented at 180° rotation. Alignment of the embedded targets was performed using the off axis DSA camera. The photoresist was 1800nm thick IX845 exposed at $250\text{mJ}/\text{cm}^2$ in i-line mode. The IX845 photoresist was coated and developed on an ACT12 track.

Metrology

Combining the two tests (single pass, and double pass) gives a reasonable method to calibrate back-to-front side overlay. The single pass test provides a means to monitor the full set of linear overlay terms, and the double pass test gives the relative mean bias between embedded target alignment and topside alignment.

Both single pass and double pass methods create overlay structures at the surface which can then be measured by a metrology tool or measured on the stepper using Stepper Self Metrology (SSM). The SSM method was specifically designed to perform stepper-to-itself overlay testing for which both layers are produced in photoresist. For optimal performance using SSM the dedicated mark design must appear identical on both layers. Figure 4 shows the SSM

mark structure. With perfect overlay, the center of layer 1 printed on the PAS 5500/750 and the center of layer 2 printed on the AP300 should coincide. Figure 4(c) shows an intentional misalignment between the layers in the X direction. This structure uses the pattern recognition capability of the stepper alignment system to measure X and Y offsets between layers. All wafers in this study were measured using SSM.

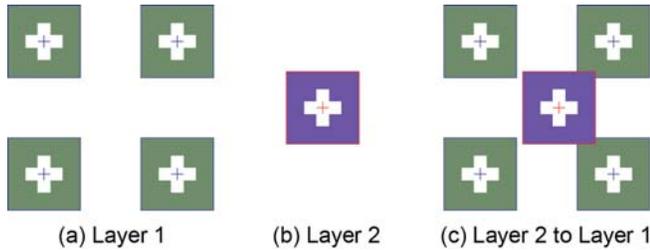


Figure 4: Stepper Self Metrology (SSM) structures (a) Layer 1, (b) Layer 2, (c) combined Layer 1 to Layer 2 with an intentional X direction offset.

For both single pass and double pass testing, the metrology sampling consists of 21 measurements per field at 11 fields on the wafer, giving a total of 231 points per wafer, as shown in figure 5.

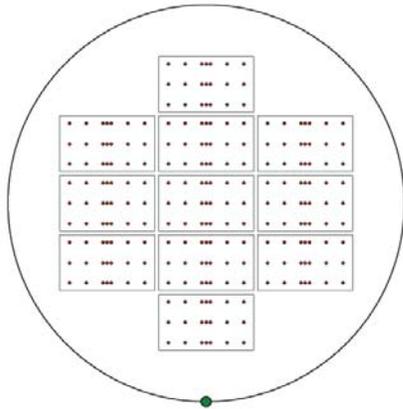


Figure 5: Overlay sampling plan on 200 mm diameter wafer consists of 21 measurements per field at 11 fields.

The main error sources that are not reflected in the single pass overlay test are errors from wafer stage Z actuation, and image degradation of the etched alignment targets viewed through silicon. These error sources can be accounted for by running the double pass test. This test aligns to embedded targets and then exposes a reference pattern in photoresist. Repeating this operation with a 180 degree rotation between passes creates a metrology structure in the photoresist that indicates twice the mean error.

All metrology tools can introduce apparent errors known as tool induced shift (TIS) [9]. These errors include asymmetries in the measurement tool interacting with the metrology mark, the materials contrast difference between

layer 1 and 2 marks, and the algorithm for localizing mark features. A standard TIS calculation involves averaging two measurements taken at 0 and 180 degrees orientation.

For the single pass topside overlay test the TIS for SSM metrology was measured to be 113 nm and 39 nm for X and Y respectively. This error is primarily attributed to the SSM measurement construction which uses a single image model to capture layer 1 in etched silicon and layer 2 targets in photoresist. The materials contrast and the CD difference between the two layers affect the TIS error measurement for single pass testing. TIS errors in single pass testing with SSM can be minimized by matching layer 1 and layer 2 dimensions in process optimization. For the double pass embedded overlay test, the material contrast and CD error sources for TIS are avoided since both layers are patterned in the same photoresist.

RESULTS AND DISCUSSION

Example image capture for embedded targets is shown in figure 6. Since CMP is an expensive process step it is important to determine if it is required for reliable target capture. Since silicon has a large index of refraction of 3.5 in the near IR, both the reflection and the visibility of surface scratches at the silicon surface will be significant. It is clear that the non-CMP wafers in 6(a) have prominent scratch mark that could interfere with pattern recognition. Since the scratch marks in 6(a) show an oriented texture that can vary in direction there is a possibility that the feature edge may be confused with texture lines if they run in the same direction. To minimize this risk, the choice of target design should be composed of a variety of angles to make the target less sensitive to texture direction such as the split circle in 6(b).

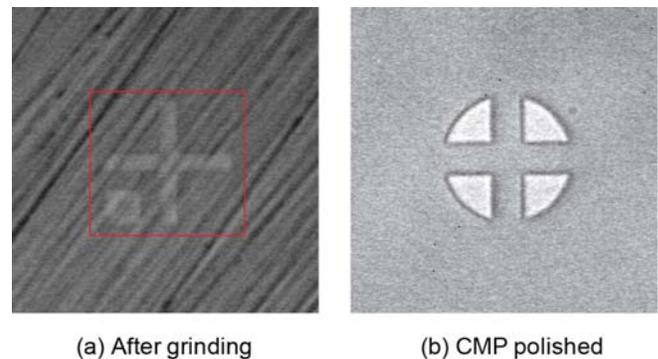


Figure 6: DSA camera view of (a) wafer after grinding, (b) wafer after grinding and CMP polish. Overall dimension of the CMP polished target is 68 μm .

In preliminary tests it is possible to repeatably capture targets in the presence of surface scratches, and this evaluation is ongoing. If miscapture can be avoided by proper setting of pattern capture criteria, then the use of redundant targets can offset a higher percentage of rejected targets.

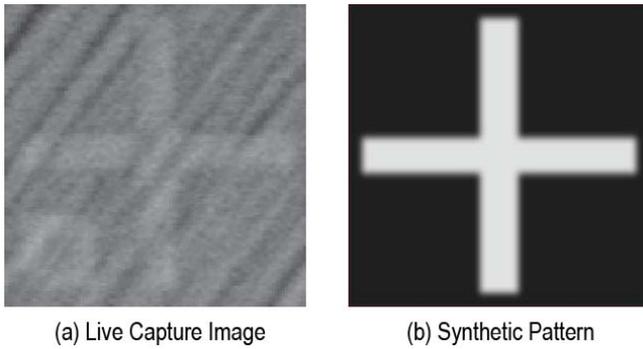


Figure 7: Live capture image (a) and synthetic pattern of the image same after grinding (b). Removing the non-repeating scratch pattern from the model significantly improves ability to recognize a target from a noisy scene.

In cases where the appearance of a target is obscured by a non-repeating pattern such as scratches, the use of a synthetically created target model helps the pattern recognition to disregard features that are non productive for pattern capture. Figure 7 shows a comparison of an actual embedded target image after grinding (a) and a matching synthetic pattern (b). A synthetic alignment target may be sufficient to avoid the requirement for a CMP step to polish the wafer surface in some cases.

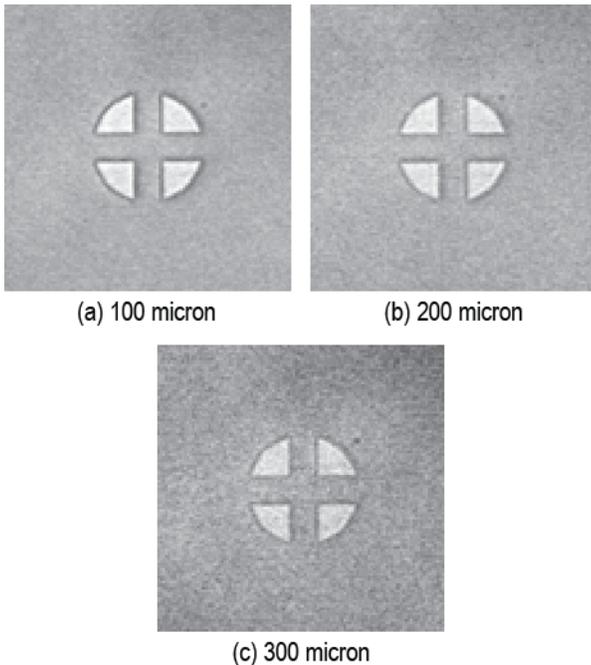


Figure 8: Images of DSA targets through three thicknesses of Si. At 300 μm the image gets grainier, but capture and overlay remain quite acceptable. Overall dimension of this target is 68 μm .

Test wafers were produced with three different thicknesses of silicon (100, 200, and 300 μm) to investigate the effectiveness of the IR DSA camera for viewing embedded metal targets under silicon. Figure 8 shows a metal target

viewed through 100, 200, and 300 μm silicon. Image quality for alignment can be maintained across this practical range of silicon thickness. Even at the thickest 300 μm thick film the target image quality was good and no problems were observed for alignment capture or overlay performance. To obtain the sharpest image, the focus system actuation in Z must have the range and precision to achieve optimum focus for different silicon thicknesses.

Overlay data taken over 15 weeks from the single pass topside test is shown in figure 9. This method uses the IR DSA camera to view targets at the wafer surface. A graph of the three sigma values is shown in figure 9(a) and a graph of the mean offset error is shown in figure 9(b). The $|\text{mean}| + 3\sigma$ overlay in both X and Y is less than 1.0 μm for every week. All overlay results are consistently less than the DSA specification of 2.0 μm . Most of this 15 week period was passive data collection except for one time when the 0.2 μm limit for adjustment was reached and means were corrected at week 11.

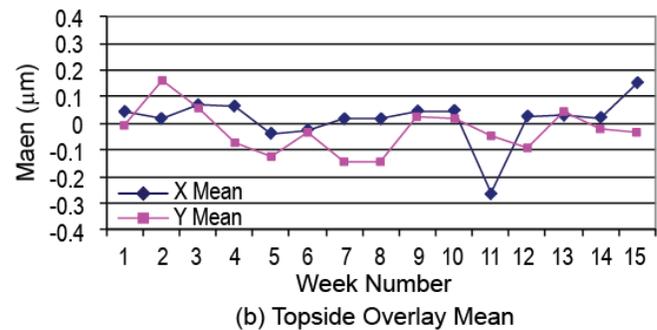
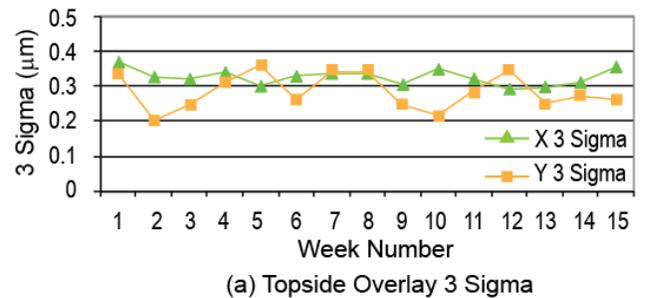


Figure 9: Plots of three sigma and mean overlay versus week number for baseline topside single pass testing using the IR DSA camera.

In figure 10, overlay means in X and Y from the double pass embedded overlay test are plotted as a function of silicon thickness. Since the double pass method will double mean errors, the data are normalized per pass by dividing the raw mean result by 2. The error bars denote ± 1 standard deviation calculated from single pass topside data shown in figure 9. The data in figure 10 shows that mean error performance is not strongly dependent on silicon thickness, which implies that the simpler single pass topside test can provide reasonable accuracy for monitoring processes that align to embedded targets.

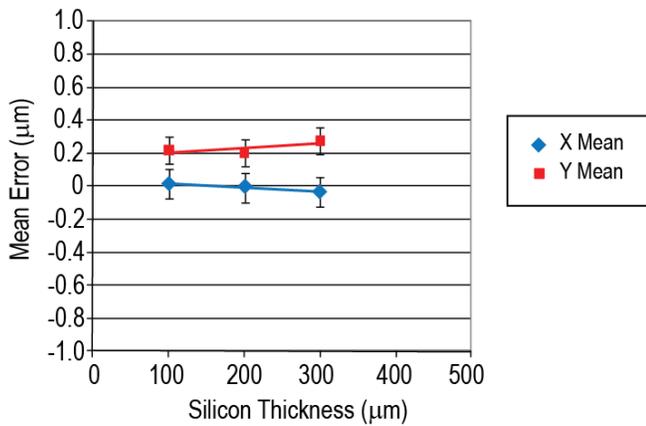


Figure 10: Plot of mean error versus silicon thickness for double pass overlay. Error bars denote ± 1 standard deviation calculated from single pass data shown in figure 9(a).

CONCLUSIONS

Test wafers with embedded Cu targets were fabricated in a variety of silicon thicknesses to evaluate the back-to-front side wafer alignment. Single pass topside overlay testing over an extended period of time shows that consistent overlay can be achieved well within the DSA specification of 2.0 μm . More detailed double pass embedded target overlay testing shows that the effect of silicon thickness does not significantly impact the mean results relative to the single pass calibration. The results show that the simpler single pass topside test can provide reasonable accuracy for monitoring processes that align to embedded targets.

Ongoing work will look at the feasibility of removing the CMP step after silicon grinding using synthetically created targets and the effect this has on back-to-front side overlay.

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